REPORT DOCUMENTATION PAGE

Form Approved
OMB NO. 0704-0188

1. AGENCY USE ONLY (Leave Blank)	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	31 March 2003	Final Technical Report 1 July 2000 – 30 June 2001

4. TITLE AND SUBTITLE
Investigation of Jet Vapor Deposited (JVD) Silicon Oxide/Nitride/Oxide (ONO) Films as Gate Dielectrics for SiC and GaN Devices

5. FUNDING NUMBERS
N00014-00-1-0831

6. AUTHOR(S)
Professor James A. Cooper, Jr.

7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)
School of Electrical and Computer Engineering
Purdue University, 465 Northwestern Ave.
West Lafayette, IN 47907-2035

8. PERFORMING ORGANIZATION REPORT NUMBER

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)
Office of Naval Research
800 North Quincy Street
Ballston Centre Tower One
Arlington, VA 22217

10. SPONSORING / MONITORING AGENCY REPORT NUMBER

11. SUPPLEMENTARY NOTES

12 a. DISTRIBUTION / AVAILABILITY STATEMENT
Approved for public release; distribution unlimited.

12 b. DISTRIBUTION CODE

13. ABSTRACT (Maximum 200 words)

Jet vapor deposited (JVD) silicon dioxide–nitride–dioxide (ONO) films are investigated as gate dielectrics for SiC MOS transistors and GaN high-electron-mobility transistors (HEMTs). The JVD process employs supersonic jets of a light carrier gas such as helium to transport depositing vapor from the source to the substrate. The high impact energies of the depositing species allow the use of room-temperature substrate, which contributes to improved film quality. JVD ONO films were deposited on n-type 4H-SiC and the electrical quality evaluated by measuring the interface state density D_{IT}. ONO films deposited without an initial nitridation process exhibited a high D_{IT} in the upper half of the bandgap, but films deposited after an initial surface nitridation in silane exhibited D_{IT} comparable to the best thermal oxides on 4H-SiC. ONO films were also deposited as gate dielectrics on GaN/AlGaN HEMTs, and the resulting devices exhibited gate-drain blocking voltages as high as 1,300V and specific on-resistances of 1.7 $m\Omega\ cm^2$.

14. SUBJECT TERMS
Oxide-nitride-oxide, ONO, Jet vapor deposition, JVD, silicon carbide, SiC, gallium nitride, GaN, high electron mobility transistors, HEMTs, high electron mobility FETs, HFETs

15. NUMBER OF PAGES
13

16. PRICE CODE

17. SECURITY CLASSIFICATION OR REPORT	18. SECURITY CLASSIFICATION ON THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
UNCLASSIFIED	**UNCLASSIFIED**	**UNCLASSIFIED**	**UL**

NSN 7540-01-280-5500

Standard Form 298 (Rev.2-89)
Prescribed by ANSI Std. 239-18
298-102

4118 095

Investigation of Jet Vapor Deposited (JVD) Silicon Oxide/Nitride/Oxide (ONO) Films as Gate Dielectrics for SiC and GaN Devices

Final Technical Report

Submitted to the

Office of Naval Research
800 N. Quincy Street
Ballston Centre Tower One
Arlington, VA 22217-560

31 March 2003

Submitted by:

James A. Cooper, Principal Investigator
School of Electrical and Computer Engineering
Purdue University, West Lafayette, IN 47906-1285

Introduction and Background

This project focused on the synthesis, characterization and application of the JVD (Jet Vapor Deposited) ONO (silicon dioxide/silicon nitride/silicon dioxide) films as high-quality, high-reliability gate dielectrics for SiC and MOSFETs and as passivation layers for AlGaN/GaN HEMTs operated at room and high temperatures (up to 350°C).

Currently, thermally grown SiO_2 is the prevailing gate dielectric for SiC. However, despite several years of effort, there remain problems with this approach, including relatively low inversion layer electron mobility (especially for 4H-SiC) , inadequate breakdown strength at high temperatures, and short operating lifetimes for n-channel enhancement-mode MOSFET's at high temperatures. At least some of the problems identified above are linked to the high density of interface traps near the conduction band in the SiO_2/SiC system [1-4]. The strong crystal-orientation dependence of the oxide growth rate on SiC is also a problem for many applications [5]. At least partly for these reasons, some researchers have replaced thermal oxide with a deposited insulator such as CVD (Chemical Vapor Deposited) silicon oxide, silicon nitride, or other insulating materials which have higher dielectric constant [6-8]. The situation for GaN is even worse, as no thermal oxide can be used as the gate dielectric, while deposited insulators, such as SiO_2, Si_3N_4, and AlN, have not shown sufficient quality to demonstrate viability.

In this project we have investigated the use of a JVD ONO stack as gate dielectric for SiC and GaN, with the goal of demonstrating high-quality, reliable dielectrics for these devices, especially at high temperatures.

Breakdown in AlGaN/GaN HEMTs is due to an avalanche process that usually occurs near the gate edge on the drain side where electric field is the most intensive. High breakdown can be achieved by inserting a layer of dielectric underneath the gate as shown in Fig. 1. The dielectric has a higher breakdown electric field than GaN (10 MV/cm for SiN and SiO_2 vs. 2 MV/cm for GaN). Higher electric field can be sustained at the drain-side gate edge in the dielectric, hence the breakdown of the HEMT is increased. This structure is called Metal-Insulator-Semiconductor (MIS) HEMT structure. The dielectric layer can also reduce the gate leakage, which mitigates the avalanche process and further increases the breakdown.

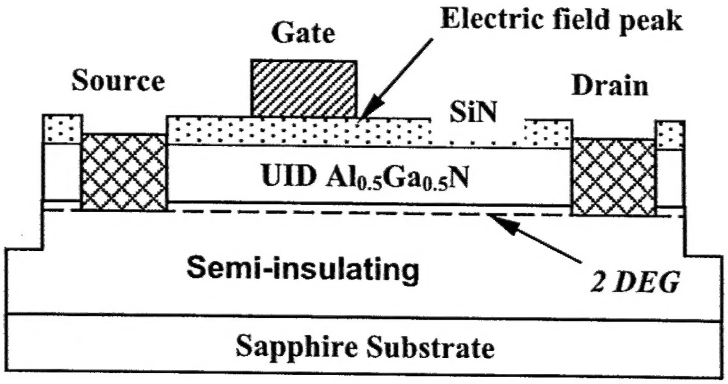

Figure 1. Metal-Insulator-Semiconductor (MIS) HEMT structure

The problems with the MIS-HEMT structure are that the transconductance of the HEMT is decreased and surface traps are introduced during the deposition of the dielectric. The JVD deposition process of Prof. T. P. Ma at Yale University offered the possibility of achieving low interface trap densities. In this project Prof. Umesh Mishra of UCSB collaborated with Prof. Ma to optimize the deposition of ONO and conventional SiN on AlGaN/GaN HEMTs. This allowed us to optimize breakdown, passivation and noise properties of this buried channel

If ultimate high frequency performance is not required, then the device can maintain a high transconductance along with a high breakdown voltage by realizing an overlapping gate structure as shown in Fig. 2. Dielectric directly under the gate is removed to maintain the same transconductance as that of a normal HEMT, while the overlapping portion of the gate keeps the peak electric field in the dielectric layer to increase the breakdown voltage.

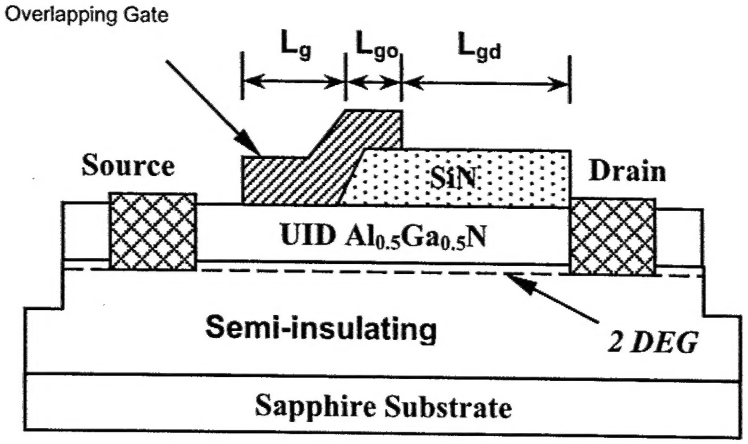

Figure 2. Overlapping gate HEMT structure.

Research has shown that Remote-Plasma PECVD can produce a high quality dielectric while keeping the surface of the sample free from plasma-related damage. Inductance Coupled Plasma (ICP) CVD is the most widely used remote plasma PECVD nowadays. Jet Vapor Deposition (JVD) is a very promising technique to make high quality dielectric with a very low level damage to the sample surface.

JVD is a novel process for synthesizing a wide variety of thin films of metals, semiconductors, and insulators [12]. It relies on supersonic jets of a light carrier gas such as helium to transport depositing vapor from the source to the substrate. Because of the separation of the constituent depositing species, and the short transit time, there is very little chance for gas-phase nucleation. The high impact energies of the depositing species allow the use of room-temperature substrate, which also contributes to the improved film quality. Other key process steps that may lead to enhanced interface quality include the pre-deposition N_2O jet cleaning, the post-deposition N_2 annealing, and the post-metallization water-vapor-annealing.

The Yale JVD SiO_2 and Si_3N_4 processes were originally developed for advanced Si CMOS applications, and these results have been published in various journals. A review article summarizes results prior to 1999 [12].

Prior to the start of this project, the Yale group had performed a few deposition runs on other semiconductors, including SiC, GaN, SiGe, GaP, and InAs, and demonstrated good quality MOS capacitors, suggesting that the JVD processes originally developed for gate dielectrics on silicon can be used as starting points for the development of gate dielectrics for other semiconductors as well. The Yale group had also made systematic studies on 6H-SiC MOS devices with JVD gate dielectrics, and the results were very encouraging. More specifically, the channel mobilities are comparable to the better SiC MOSFET's published in the literature, while the operating lifetimes of N-channel MOSFET's, as determined by Time-Dependent Dielectric Breakdown (TDDB) data, were orders of magnitude longer than the best reported data for SiC MOSFET's at elevated temperatures (above 300°C). In fact, the best reported lifetime value for state-of-the-art SiC MOSFET's was less than 300 hours at 350°C [8], which is far from the 10-year lifetime requirement for many applications. In contrast, the lifetimes of JVD SiC MOSFET's was projected to be over 200 years at temperatures as high as 450°C [11]. The improved lifetimes of JVD devices are consistent with reduced gate leakage currents, higher dielectric breakdown field strengths, and reduced dielectric charge and interface traps.

In the following sections, we summarize the results obtained for JVD ONO films deposited on silicon carbide and on GaN. The SiC work involves optimization of film quality using feedback from electrical characterization of MOS capacitors, since these structures could be fabricated and analyzed quickly, permitting rapid feedback to the deposition experiments. This approach allowed us to try many different experimental conditions, leading to very effective optimization of film quality. The resultant film quality is compared to SiC MOS capacitors with dielectric films formed by thermal oxidation and subsequent nitridation in NO, representing the current state-of-the-art in SiC MOS quality. As will be seen, the JVD ONO films resulting from our optimized depositions were of comparable interface quality to the best thermal oxides yet reported. In addition, these films avoid problems with anisotropy of thermal oxidation, and provide longer lifetimes under high-temperature and high-field stressing. The GaN experiments involved inserting ONO films as gate dielectrics in GaN/AlGaN HEMTS. The ONO dielectric films increased gate-to-drain breakdown voltage into the low kilovolt range, opening the possibility of using GaN HEMTS for high frequency power supply applications.

References

1. T.Ouisse, N.Becourt, F.Templier and C.Jaussaud, *J. Appl. Phys.* 75 (1), p.604,1994.
2. C-M.Zetterling and M.Ostling, *Diamond, SiC and Nitride Wide Bandgap Semiconductors*, 339, eds. C.H.Carter, Jr. G.Gildenblatt, S.Nakamura and R.J.Nemanich (Pittsburgh, PA: Materials Research Society,1994) p.209, 1994.
3. D.M. Brown, et.al,, *IEEE Trans on Electron Dev.* 41(4), p.618, 1994.
4. A. K. Agarwal, et al, *Proc. 8th Int. Symposium on Power Semiconductor Devices & ICs*, p.119, 1996.
5. J. N. Shenoy, M. K. Das, J. A. Cooper, Jr., M. R. Melloch, and J. W. Palmour, *J. Appl. Phys.* 79(6), p.3042, 1996.
6. T. Billon, E. Bano, L. Cioccio, T. Ouisse, P. Lassagne, and C. Jaussaud, *Microel. Eng.*28, p.193, 1995.
7. J. J. Kopanski and G. P. Carver, presented at *The South NCSU National Review Meeting on the Growth and Characterization of SiC and its Employment in Semiconductor Applications*, NCSU, October 1987.
8. L. A. Lipkin, and J. W. Palmour, *IEEE Trans. on Electron Dev.* 46(3), p.525, 1999.
9. L. A. Lipkin *et al, J. of Electronic Materials* vol. 25, no.5, p.909, 1996.
10. Xiewen Wang, Z.J. Luo, and T.P. Ma, *IEEE Trans. on Electron Dev.* 47(2), 458, 2000.
0. X.W. Wang, W.J. Zhu, X. Guo, T.P. Ma, and M. Rao, paper 8.7 in *Technical Digest* of *International Electron Device Meeting*, Washington, DC, December 5-8, 1999.
1. T.P. MA, *IEEE Trans. Electron Devices*, vol.45(3), p. 680, 1998.

Electrical Characteristics of Jet-Vapor-Deposited Oxide-Nitride-Oxide Dielectric Films on Silicon Carbide

Department of Electrical Engineering
Yale University, New Haven, CT
and
School of Electrical and Computer Engineering
Purdue University, West Lafayette, IN

The following results are based on MIS capacitors with ONOn stack gate dielectric deposited on 4H-SiC, where the ONO stands for the Oxide-Nitride-Oxide stack that we had previously developed for 6H-SiC, and the lower-case n stands for the ultra-thin nitride layer at the SiO_2/4H-SiC interface.

Figure 1 shows the effect of nitrogen incorporation on the CV characteristics of 4H-SiC MIS capacitors. There are 4 sets of multi-frequency CV curves in Fig.1. Set A is from a control ONO gate stack without the interfacial nitride layer (or n-layer), while sets B, C and D are from ONOn stacks with the n-layer fabricated at different silane flow rates. It is clearly seen that without nitrogen at the interface, the control sample shows large flatband voltage shift and frequency dispersion, indicating a high density of interface traps. By adding the ultra-thin n-layer on the SiC surface, the frequency dispersion decreases systematically as the SiH_4 flow rate was decreased from 2 to 0.6 sccm, and the n-layer deposited with a SiH_4 flow rate of 0.6 sccm yielded the best D_{it} data (see the D set of curves). A further decrease of the SiH_4 flow rate caused the C-V curves to degrade again, as manifested in the increased stretch-out and larger frequency dispersion near strong accumulation. The trend shown in Fig.1 suggests that a finite amount of silicon is necessary at the interface to realize the beneficial nitrogen effect, but excessive amounts of silicon tend to reduce the beneficial nitrogen passivation effect. Shown in Fig. 2 are D_{it} distributions of our JVD ONO and ONOn samples along with some published D_{it} data for comparison. As indicated by the solid triangles in Fig.2, our previous JVD ONO stack yielded D_{it} values no better than those samples made of conventional thermal SiO_2 even though its reliability far exceeded the state-of-the-art [1]. However, with an ultra-thin silicon nitride layer added at the SiO_2/SiC interface, the D_{it} values in the energy range of 0.1 - 0.2eV below the 4H-SiC conduction band are decreased over an order of magnitude, to $1x10^{12}/cm^2$-eV or below. These are among the lowest D_{it} values in this energy range yet reported for 4H-SiC, and are comparable to the best results obtained using conventional thermal oxidation followed by NO annealing [2].

ARXPS studies confirmed the presence of nitrogen at the SiO_2/4H-SiC interface, as evidenced by the well-defined N-1s peak (shown in Fig. 3) with the binding energy centered at 397.7eV as the sampling depth reaches the ONOn /4H-SiC interface. The total atomic concentration of nitrogen is estimated at 3.1 at%. The Si-2p binding energy of 101.5eV (the small peak shown in Fig. 4a) originated from the interfacial silicon nitride layer, in conjunction with the N-1s binding energy of 397.7eV suggests that such deposited interfacial nitride layer is near its stoichiometric form of Si_3N_4 [3]. We speculate that one of the beneficial effects of nitrogen incorporation at the SiO_2/SiC interface may arise from reduced silicon sub-oxides. This speculation is supported by the fact that the Si-2p spectra taken on the control sample (shown in Fig.4b) exhibit multiple components, indicative of silicon sub-oxides formed at the SiO_2/SiC interface. The ARXPS data also showed some evidence of N passivation of carbon dangling bonds, although further investigation along this line is required.

In summary, we have demonstrated significant reduction of interface-trap density in the upper half of the band gap by adding an ultra-thin layer of silicon nitride before gate oxide deposition. We believe that this reduction is related to the presence of nitrogen at the SiO_2/SiC interface. Although the exact mechanism remains to be studied, it is likely to be a result of reduced sub-oxides formation, as well as passivation of silicon and carbon dangling bonds at the interface.

References

1. X.W. Wang, W. Zhu, X. Guo, and T.P. Ma, Technical Digest of International Electron Devices Meeting, p. 209, 1999.
2. G.Y. Chung, C.C. Tin, J.R. Williams, et al., IEEE Electron Device Lett., vol.22, pp.176-178, 2001.
3. John Moulder *et.al.*, "Handbook of X-ray Photoelectron Spectroscopy", Physical Electronics, 1992.

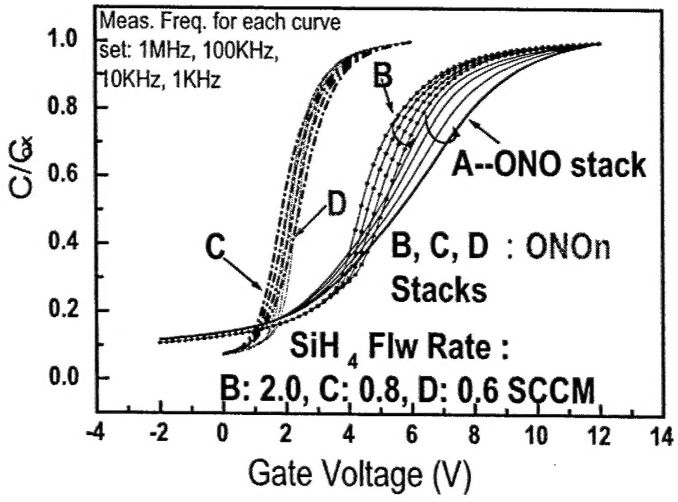

Figure 1. Multi-frequency CV curves taken on (A) the control ONO stack, and on (B, C, D) ONOn stacks with various SiH_4 flow rates during the interfacial ultra-thin nitride layer deposition.

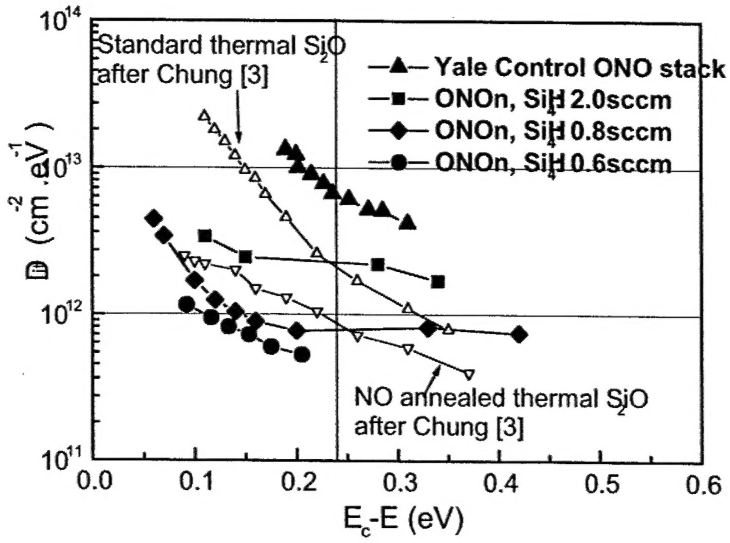

Figure 2. D_{it} distributions for JVD ONO control and ONOn samples with variable SiH_4 flow rate for the ultra-thin silicon nitride layer. Open symbols are reference data after Chung [14].

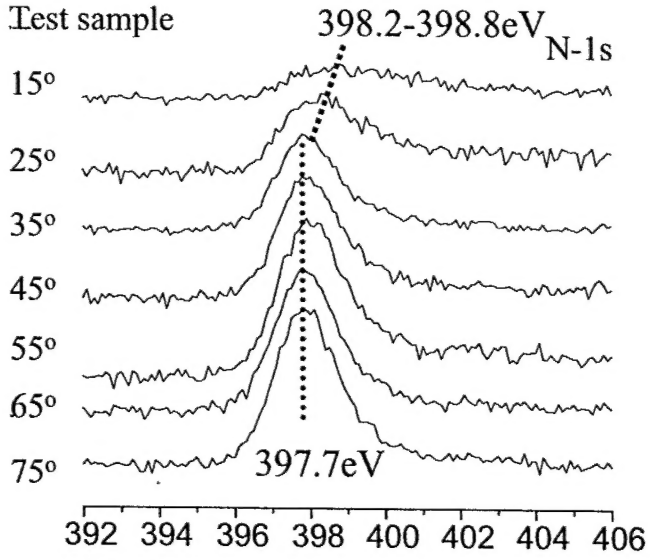

Figure 3. ARXPS N-1s spectra taken on a ONOn stack from the most grazing (15°) to almost normal to the sample surface (75°).

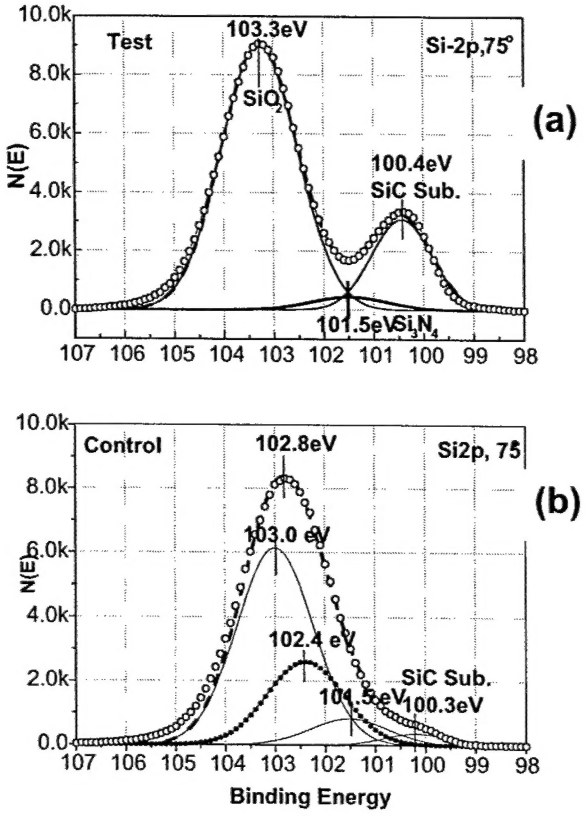

Figure 4. Si-2p spectra on (a) ONOn/SiC and (b) ONO/SiC control sample, respectively, at 75°. Open circles represent experimental XPS data, the connecting dotted curves are from curve fitting, and the solid curves are the best-fit components. The multiple fitting components in (b) indicate sub-oxides in the control sample.

Fabrication of Metal-Insulator-Semiconductor (MIS) HEMT Structures

Final report for PURDUE

Department of Electrical and Computer Engineering
University of California, Santa Barbara, CA 93106

ABSTRACT

Previous work has shown great reduction of gate leakage by utilizing MIS structure. We report here our research on using gate dielectrics to increase breakdown voltage of GaN HEMTs. A GaN MIS HEMT with JVD SiO_2 as the gate dielectric was fabricated, displaying a breakdown voltage of 1300V with a specific on-resistance of 1.7 $m\Omega \cdot cm^2$. A nitride-oxide-Nitride gate dielectric scheme has been investigated to achieve high switching speed while maintaining breakdown voltage in the kilo-volts range. Optimization of the MIS HEMT for power supply applications is discussed at the end of the report.

HIGH VOLTAGE PERFORMANCE OF GaN MIS HEMTs

GaN epi-layers were grown on semi-insulating SiC substrate by MOCVD (Metal Organic Chemical Vapor Deposition). There are two reasons to use a SiC substrate. First, as opposed to a Sapphire substrate, there is no out-diffusion of shallow donor (O_2) for growth on SiC. It is much easier to grow semi-insulating GaN buffer layer on SiC than on sapphire substrate for high voltage applications. The other reason is that the thermal conductivity of SiC is four times higher than that of sapphire. Calculation shows that the temperature rise for HEMTs on sapphire substrate can be 10 times higher in comparison with that for HEMTs on SiC substrate [1]. This advantage of SiC substrate is highly desired when we operate GaN HEMTs at elevated temperature and with ultra-high power density.

An 85-nm AlN layer growth on SiC was followed by the deposition of 1 μm un-intentionally doped GaN layer grown at low pressure, 30-nm GaN layer grown at high pressure, and finally capped with 16-nm $Al_{.27}Ga_{.73}N$ barrier layer. Hall measurement showed electron sheet concentration $n_s = 9.54\times10^{12}$ cm^{-2} and mobility $\mu_n = 1280$ $cm^2/V\cdot s$ even though there was no intentional doping in the whole material system. The MIS HEMT structure is shown in Fig. 1. The dielectric underneath the gate helps reduce gate leakage under high drain bias, thus alleviates the leakage assisted impact ionization and increases breakdown voltage. The SiO_2 film was deposited in Yale University by Jet Vapor Deposition (JVD) before device processing. JVD SiO_2 is proven to have very high breakdown electric field strength (≥ 12 MV/cm) with low leakage current [2] even at 450 °C. C-V measurement revealed that the SiO_2 film forms deep surface traps on AlGaN in

the mid-bandgap. Our measurement showed 2 to 4 orders lower leakage with this MIS structure than without gate dielectric. Ti/Al/Ni/Au of 220/2000/550/450 Å was annealed at 870 °C to make ohmic contact and Ni/Au was used as the gate metal. Device process was finished with RIE (Reactive Ion Etch) mesa isolation. Devices with different gate lengths (L_g = 0.5 ~ 4 μm), gate-drain distances (L_{gd} = 4 ~ 20 μm) and gate width (W_g = 500 & 1,000 μm) were fabricated.

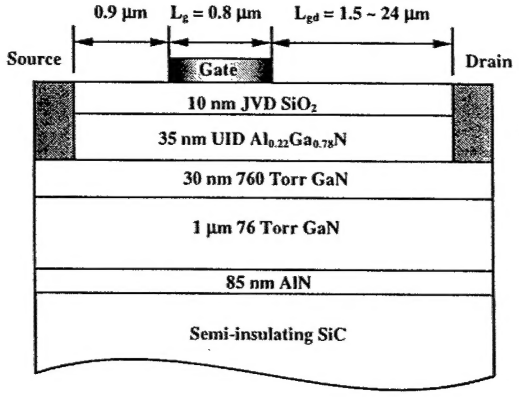

Figure 1. Schematic diagram of epitaxial layers and cross sections of insulated-gate GaN HEMT with JVD SiO_2

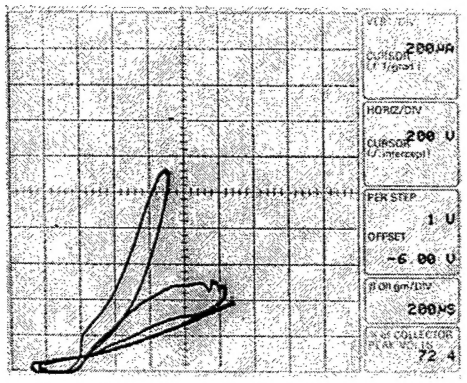

Figure 2. Breakdown characteristics of a high breakdown GaN HEMT with gate to drain spacing of 16 μm

The I_{DS} - V_{DS} characteristics for a GaN HEMT with L_g = 1 μm, L_{gd} = 16 μm and W_g = 500 μm are shown in Fig. 2 and Fig. 3. The breakdown voltage of this device is 1300 V, a remarkable improvement from previous reported best value of 570 V [3]. The specific on-resistance is 1.7 mΩ·cm^2 (active area ~ 9.25×10^{-5} cm^2) with gate bias of 0 V (R_{on} can also be expressed as 9.1 Ω·mm for lateral device). The breakdown voltage is by far the highest value achieved on all devices based on GaN material, and the on-resistance is lower than any SiC switching devices. The power device figure of merit V_{BR}^2 / R_{on} = 9.94×10^8 [V^2·Ω^{-1}cm^{-2}] is also higher than any kind of switching devices reported, and this number approaches the SiC limit shown in Fig. 4.

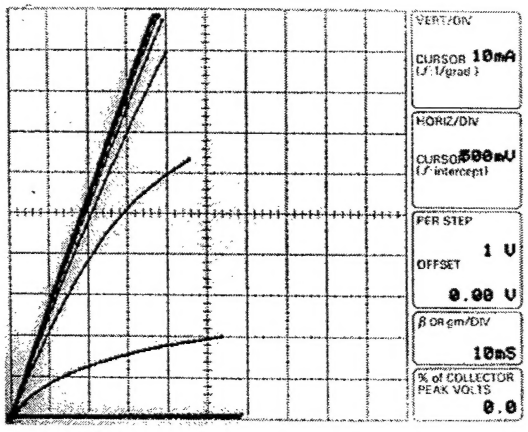

Figure 3. Low bias I_{ds}-V_{ds} characteristics of the high breakdown GaN HEMT

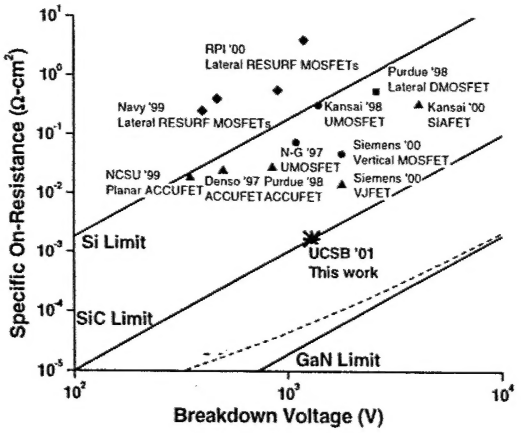

Figure 4. Comparison of Si, SiC and GaN devices on the relationship between the on-resistance and the breakdown voltage

The threshold voltage is –9 V and $\Delta V_{DS} / \Delta V_{GS} \approx 140$. This high ratio is highly preferred in low-voltage controlled high-voltage applications. TLM pattern measurement showed ohmic contact resistance of 0.8 Ω·mm and channel resistance of 7.5 Ω·mm (or 400 Ω·□). With precise device layout design and improved ohmic contacts, the on-resistance could drop to 0.9 mΩ·cm^2. There is source-drain leakage when the L_{gd} shorter than 8 μm due to channel punch-through and space-charge limited current, while devices with longer L_{gd} showed destructive breakdown. The breakdown voltage increases with longer gate to drain distance and saturates at $L_{gd} = 12 \sim 16$ μm.

SWITCHING SPEED

I_{DS} - V_{DS} curves measured under pulsed conditions were compared with DC measurement. The period of the gate bias pulse is 67 milli-second and the pulse width is 80 micro-second. The pulsed current level is much lower than the DC measurement. The discrepancy between DC and pulse measurement is referred to "dispersion" in microwave power electronics. Pulse measurement is an indirect way to probe the device switching speed. If the device is turned-on at a speed higher than the pulse, the current that can pass the switch will be limited by the pulsed current level (much lower than the DC current level). Longer pulse width is needed to fully recover the drain current. 80 μs pulse implies the switching speed of this device is slower than 6.25 KHz.

Dispersion is caused by deep traps in the material, especially the surface traps. Under reverse gate bias (turn-off), the electrons from gate are injected into the surface traps between gate and drain, and the channel is depleted by the trapped electrons. When the device switches to forward bias (turn-on), those trapped electrons should emit from the traps and let current pass through the channel. If the traps are deep, the emission process is considerably slow, resulting slow channel current recovery, or slow switching speed. C-V measurement revealed that the SiO_2 film forms deep surface traps on GaN in the mid-bandgap (time constant can be as long as seconds). Experiments on microwave power HEMTs have shown substantial improvement of dispersion by SiN surface passivation. SiN may be also a good choice for gate dielectric.

Devices were then fabricated with JVD SiN gate dielectric (Fig. 5 (a)). The devices with SiN gate dielectric showed less than 5% dispersion, implying its high switching speed. However, the breakdown voltage of these devices was only about 500 V. Gate diode measurement showed larger leakage current compared to normal GaN HEMTs without gate dielectric as shown in Fig. 6. The breakdown voltage is believed to be lowered by the leakage enhance impact ionization. It is crucial to maintain both low gate leakage and effective passivation on AlGaN to achieve both high breakdown voltage and high switching speed. To do this, SiO_2 was deposited only under the gate and other channel region was passivated by SiN (Fig. 5 (b)). The gate leakage dropped to 4 orders lower, but significant dispersion (75%) was still observed in the pulsed measurement. This shows that the deep traps beneath the SiO_2 under the gate still cause dispersion.

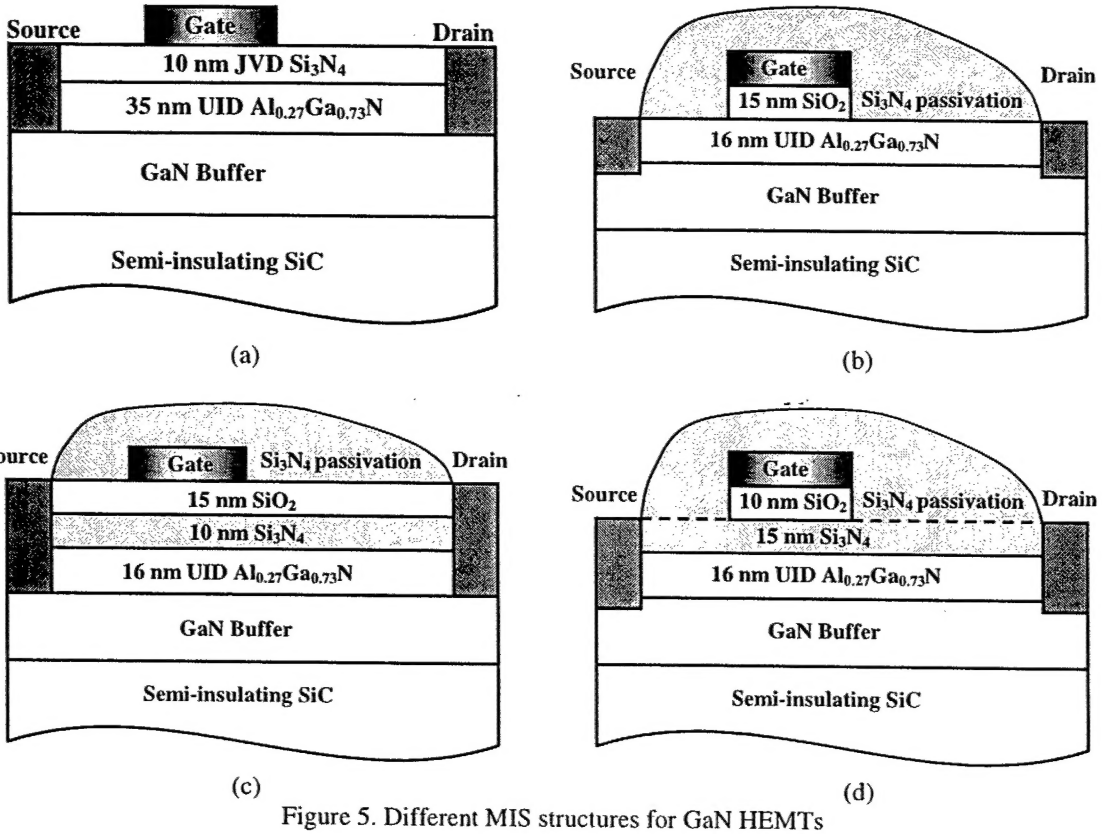

Figure 5. Different MIS structures for GaN HEMTs

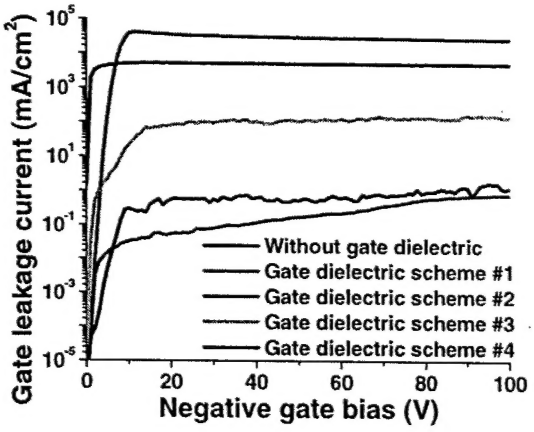

Figure 6. Gate leakage measurement of the four insulated gate GaN HEMT schemes

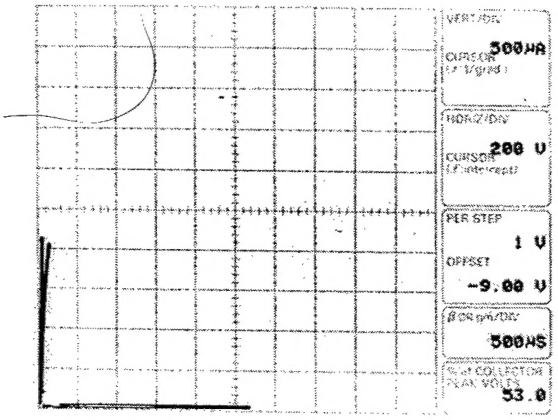

Figure 7. Breakdown characteristics of the insulated gate GaN HEMT schemes #4

The third gate dielectric scheme is the SiO_2/SiN double layer as shown in Fig. 5 (c). The bottom SiN layer forms good AlGaN surface while the top SiO_2 layer helps to reduce the gate leakage. The dispersion from this scheme was improved greatly but still noticeable (44%). It was suspected that the top SiO_2 layer limited the commutation of the electrons between the gate and the SiN/AlGaN interface traps, causing slow response of the traps. To prevent this side effect, the double-layer gate dielectric scheme was modified into Fig. 5 (d). A thin layer SiN was first applied all over the device, then the second SiO_2 layer

was only deposited under the gate, and the device was finished with thick, planar SiN passivation. The dispersion from this device was neglectable (< 10%) with greatly compressed gate leakage (nearly four orders lower than that of normal GaN HEMTs and comparable to the best insulated gate scheme as shown in Fig. 6). As a result, the breakdown voltage of this device still exceeded 1000 V as exhibited in Fig. 7. No hysteresis was observed in the I-V curves as compared to Fig. 2, which is another indication of low dispersion and high switching speed.

CONCLUSIONS

GaN HEMT with 1.3 KV breakdown voltage and very low on-resistance of 1.7 $m\Omega \cdot cm^2$ were realized on an MIS HEMT structure grown on semi-insulating SiC substrate. The state-of-art power device figure of merit of V_{BR}^2/R_{on} = 9.94×10^8 $[V^2 \cdot \Omega^{-1} cm^{-2}]$ was achieved on this device. Different insulated gate schemes were investigated to increase the switching speed while maintain high breakdown voltage. Base on the analysis and experiments, GaN HEMTs are a promising choice for low loss, high voltage switching devices working at high temperature environment.

More and more research groups have found that the SiN passivation can eliminate dispersion from GaN HEMTs, but the mechanism is still unclear. Further work has to be done to understand the interaction between the SiN and AlGaN layers.

Simulations [4] have shown that using a field plate with the gate will increase breakdown voltage by 4 times higher than without such a field plate at a channel electron density of 1.5×10^{13} cm^{-2}. Combined MIS and field plate HEMT structure should be able to provide us both high breakdown voltage and high switching speed. While simulations require about 1 μm dielectric for field plate to take effect, JVD only deposits dielectric up to 100 nm. It is suggested to use ICP-PECVD to deposit thick high quality SiN with JVD SiO_2 under the gate to take the advantage of field plate.

REFERENCES

[1] R. Gaska, Q. Chen, J. Yang, A. Osinsky, M. A. Khan, and M. S. Shur, "High-temperature performance of AlGaN/GaN HFET's on SiC substrate," *IEEE Electron Devices Letters*, vol. **18**, pp. 492-494, 1997.

[2] B. Gaffey, L. J. Guido, X. W. Wang, and T. P. Ma, "High-quality oxide/nitride/oxide gate insulator for GaN MIS structures," *IEEE Transactions on Electron Devices*, vol. **48**, pp. 458-464, 2000.

[3] N.-Q. Zhang, S. Keller, G. Parish, S. Heikman, S. P. DenBaars, and U. K. Mishra, "High breakdown GaN HEMT with overlapping gate structure," *IEEE Electron Device Letters*, vol. **21**, pp. 421-423, 2000.

[4] S. Karmalkar and U. K. Mishra, "Enhancement of breakdown voltage in AlGaN/GaN HEMTs using a field plate," *submitted to IEEE Transactions on Electron Devices*, 2000.

[5] B. J. Baliga, *Power Semiconductors Devices*: PWS Publishing Company, 1996.